1.	Course title	Hardware Description Languages		
2.	Course code			
3.	Study program	KNI		
4.	Unit offering the course	**FCSE**		
5.	Undergraduate/postgraduate/PhD	**Undergraduate**		
6.	Year/semester 2/summer (elective)	7. ECTS: **6**		
8.	Teacher(s)	assoc. prof. d-r Dimitar Trajanov, assist. prof. d-r Igor Miskovski		
9.	Course prerequisites			
10.	Goals (competences): Get introduced to hardware description languages: SystemC, VHDL and Verilog. To use hardware description languages for synthesis of logic circuits in the automated digital design. Understand the process of synthesis of digital integrated circuit, starting from HDL code up to the Field programmable gate array.			
11.	Course content: VHDL, Verilog and SystemC, functional and structural description, simulation, synthesis, programming the FPGA, placement and routing of IC masks, test bench simulations. Introduction to design methodologies using hardware description languages. Structural, concurrent and sequential VHDL descriptions, subprograms, VHDL operators, signals and variables, types of variables, the WAIT command and sensitivity list. Simulation of VHDL / Verilog models, test models, debugging in the console. Design, organization and parameterization: subprograms, packages, fixed and generic parameters, design configuration, general tests. Modelling delays and time problems. Data flow in VHDL / Verilog: multiplexers, finite automata.			
12.	Teaching methods: Lectures supported by slide presentations, interactive lectures, trainings (using lab equipment and software packages), team work, case studies, invited guests and lectures, individual practical assignments presentations, seminar paper, e-learning (forums, consultations).			
13.	Total available time	6 ECTS x 30 hours = 180 hours		
14.	Distribution of the available time	30 + 45 + 105 = 180 hours		
15.	Teaching activities	15.1.	Lectures	30 hours
		15.2.	Training (labs, problem solving), seminar and team work	45 hours
16.	Other activities	16.1.	Project work	30 hours
		16.2.	Self study	25 hours
		16.3.	Home work	50 hours
17.	Grading			
	17.1.	Tests		70 points
	17.2.	Seminar work/project (written or oral presentation)		20 points

	17.3.	Active participation			10 points	
18.	Grading criteria			to 50 points	5 (five) (F)	
				from 51 to 60 points	6 (six) (E)	
				from 61 to 70 points	7 (seven) (D)	
				from 71 to 80 points	8 (eight) (C)	
				from 81 to 90 points	9 (nine) (B)	
				from 91 to 100 points	10 (ten) (A)	
19.	Final exam prerequisites		Completed activities 15.1 and 15.2			
20.	Course language		Macedonian and English			
21.	Quality assurance methods		Internal evaluation and student polls			
22.	Literature					
	22.1.	Compulsory				
		No.	Authors	Title	Publisher	Year
		1.	John Williams	Digital VLSI Design with Verilog	Springer	2008
		2.	Mark Zwolinski	Digital System Design with VHDL 2nd Edition	Pearson Education	2008
		3.	David C. Black and Jack Donovan	SystemC: FROM THE GROUND UP	Kluwer Academic Publishers	2004
	22.2.	Additional				
		No.	Authors	Title	Publisher	Year
		1.	Roth Charles H., John Lizy Kurian	Digital Systems Design using VHDL	Thomson	2009
		2.	Michael D. Ciletti	Advanced Digital Design with Verilog 2e	Prentice Hall	2010
		3.	J. Bhasker	A SystemC Primer, 2nd edition	Star Galaxy Publishing	2010