1.	Course title	**Embedded software design in ASIC and FPGA**		
2.	Course code	SOCD-I-01		
3.	Study program	**System on Chip Design**		
4.	Unit offering the course	**FCSE**		
5.	Undergraduate/master/PhD	**Master**		
6.	Year/semester 1(2)/winter/elective	7. ECTS: **6**		
8.	Teacher(s)	Assist. Prof. Lasko Basnarkov		
9.	Course prerequisites	None		
10.	Goals (competences): After successfully completing the course, the student is expected to understand the logic/FSM and be able to implement embedded hardware in SoC architecture such as ASIC or FPGA. The implementation methodology used will be based on high-level logic and synthesis.			
11.	Course content: Logical/FSM synthesis and design concepts. HDL coding systems for efficiency, simulation, timing, energy efficiency and congestion aware. Technological and optimization problems. Optimised designs concerning surface area, performances, energy consumption using logical/FSM synthesis. Static timing analysis. High-level synthesis concepts. Scheduling, allocation, connecting, storage, interconnections and control synthesis. Hardware acceleration. Design space exploration. Hardware and software partitioning.			
12.	Teaching methods: Lectures supported by slide presentations, interactive lectures, trainings (using lab equipment and software packages), team work, case studies, invited guests and lectures, individual practical assignments presentations, seminar paper, e-learning (forums, consultations).			
13.	Total available time	6 ECTS x 30 hours = 180 hours		
14.	Distribution of the available time	30 + 15 + 135 = 180 hours		
15.	Teaching activities	15.1.	Lectures	30 hours
		15.2.	Training (labs, problem solving), seminar and team work	15 hours
16.	Other activities	16.1.	Project work	60 hours
		16.2.	Self study	25 hours
		16.3.	Home work	50 hours
17.	Grading			
	17.1.	Tests		50 points
	17.2.	Seminar work/project (written or oral presentation)		35 points
	17.3.	Active participation		15 points
18.	Grading criteria	to 59 points		5 (five) (F)
		from 60 to 68 points		6 (six) (E)
		from 69 to 76 points		7 (seven) (D)
		from 77 to 84 points		8 (eight) (C)

				from 85 to 92 points		9 (nine) (B)
				from 93 to 100 points		10 (ten) (A)
19.	Final exam prerequisites			Successfully completed activities 15.1 and 15.2		
20.	Course language			Macedonian and English		
21.	Quality assurance methods			Internal evaluation and student questionnaires		
22.	Literature					
	22.1.	Compulsory				
		No.	Authors	Title	Publisher	Year
		1.	Sanjay Churiwala and Sapan Garg	Principles of VLSI RTL Design	Springer	2008
		2.	Lee Weng Fook	VLIW Microprocessor Hardware Design: On ASIC and FPGA	McGraw-Hill Professional	2007
		3.	Ronald Sass	Embedded Systems Design with Platform FPGAs: Principles and Practices	Morgan Kaufmann	2010
	22.2.	Additional				
		No.	Authors	Title	Publisher	Year
		1.		Selected papers		
		2.				
		3.				