1.	Course title	**Design using HDL languages**		
2.	Course code	SOCD-I-02		
3.	Study program	**System on Chip Design**		
4.	Unit offering the course	**FCSE**		
5.	Undergraduate/master/PhD	**Master**		
6.	Year/semester 1(2)/winter/elective	7. ECTS: **6**		
8.	Teacher(s)	Assist. Prof. Igor Mishkovski		
9.	Course prerequisites	None		
10.	Goals (competences): After successfully completing the course, the student is expected to: model digital hardware using HDL, name and describe different phases of the digital hardware design process, be familiar with several types of target architectures, design digital hardware, use typical design techniques for synchronized and asynchrony machines.			
11.	Course content: Introduction to HDL languages. System modelling using VHDL. VHDL alternatives. Introduction to VHDL-AMS. Combinatorial and sequential component design. Target architectures. FPGA synthesis. Synchronized vs asynchrony machines. Microcontrollers and data buses.			
12.	Teaching methods: Lectures supported by slide presentations, interactive lectures, trainings (using lab equipment and software packages), team work, case studies, invited guests and lectures, individual practical assignments presentations, seminar paper, e-learning (forums, consultations).			
13.	Total available time	6 ECTS x 30 hours = 180 hours		
14.	Distribution of the available time	30 + 15 + 135 = 180 hours		
15.	Teaching activities	15.1.	Lectures	30 hours
		15.2.	Training (labs, problem solving), seminar and team work	15 hours
16.	Other activities	16.1.	Project work	60 hours
		16.2.	Self study	25 hours
		16.3.	Home work	50 hours
17.	Grading			
	17.1.	Tests		50 points
	17.2.	Seminar work/project (written or oral presentation)		35 points
	17.3.	Active participation		15 points
18.	Grading criteria		to 59 points	5 (five) (F)
			from 60 to 68 points	6 (six) (E)
			from 69 to 76 points	7 (seven) (D)
			from 77 to 84 points	8 (eight) (C)
			from 85 to 92 points	9 (nine) (B)
			from 93 to 100 points	10 (ten) (A)

19.	Final exam prerequisites			Successfully completed activities 15.1 and 15.2		
20.	Course language			Macedonian and English		
21.	Quality assurance methods			Internal evaluation and student questionnaires		
22.	Literature					
	22.1.	Compulsory				
		No.	Authors	Title	Publisher	Year
		1.	Frank Vahid, Roman Lysecky	VHDL for Digital Design	Wiley; 1 edition	2007
		2.	Igor Mishkovski, Sonja Filiposka, Dimitar Trajanov, Aksenti grnarov	Designing SoC using SystemC, Skopje		2009
		3.	Sasho Gramatikov, Igor Mishkovski, Sonja Filiposka, Dimitar Trajanov, Aksenti Grnarov	Designing SoC using VHDL		2009
	22.2.	Additional				
		No.	Authors	Title	Publisher	Year
		1.		Selected papers		
		2.				
		3.				